

FIG. 1

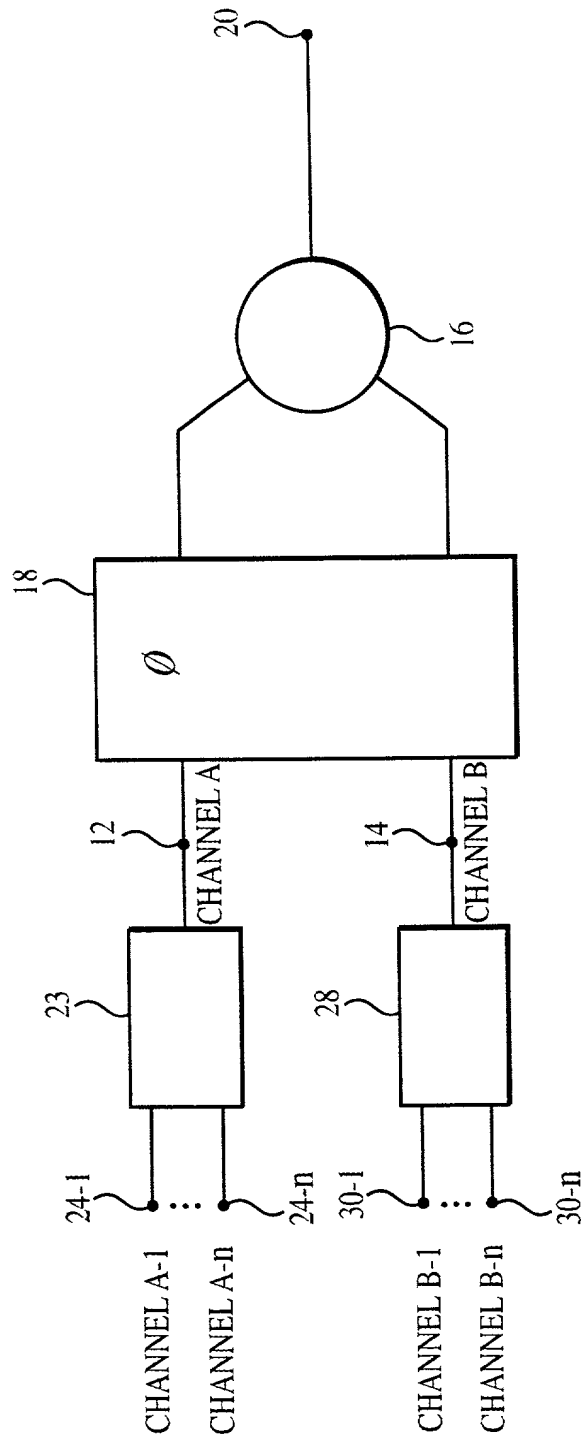


FIG. 2a

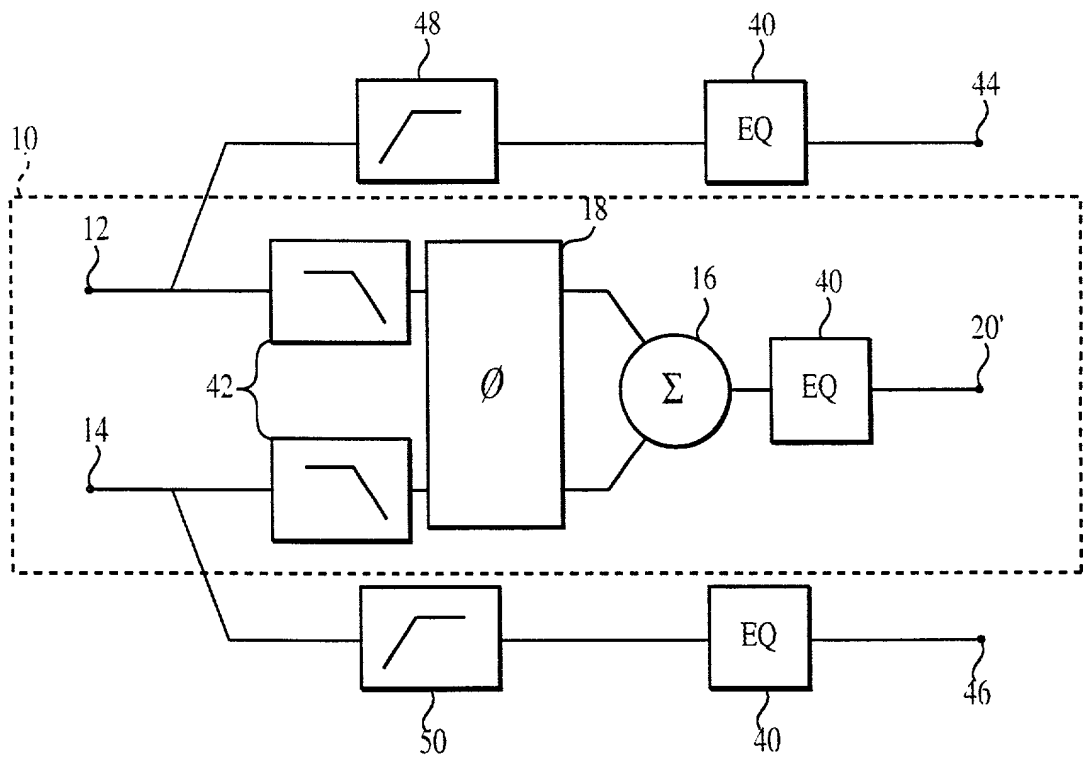


FIG. 3a

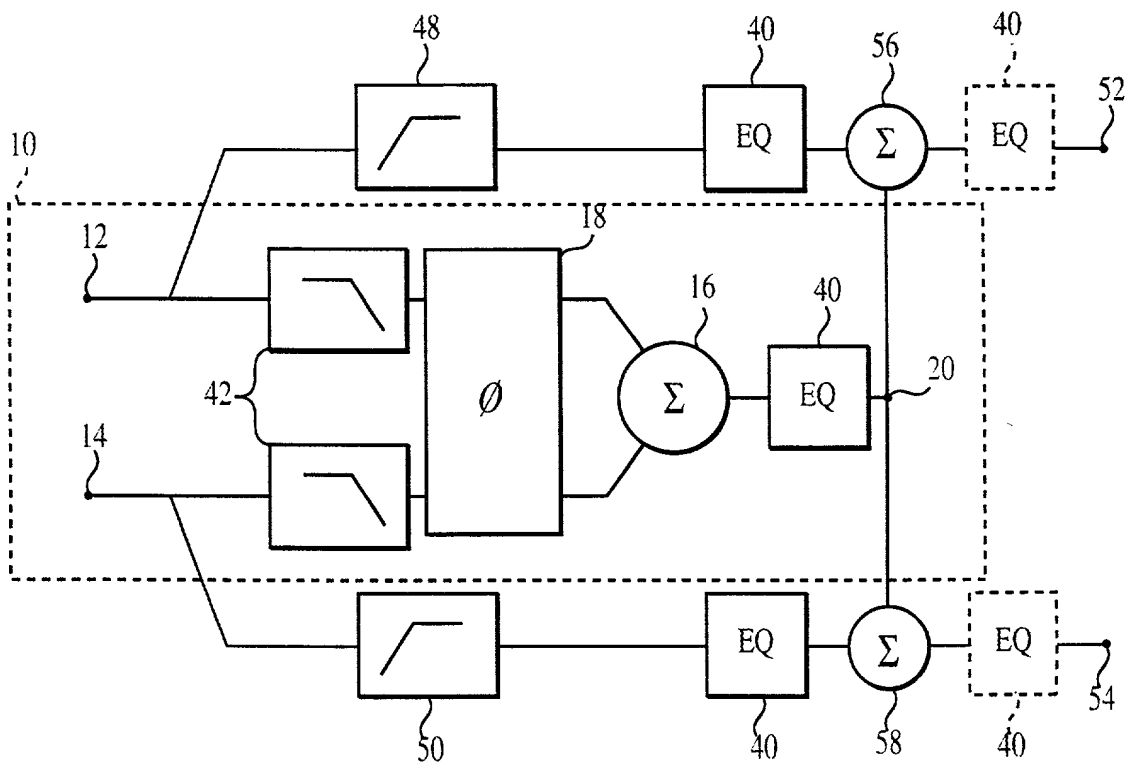


FIG. 3b

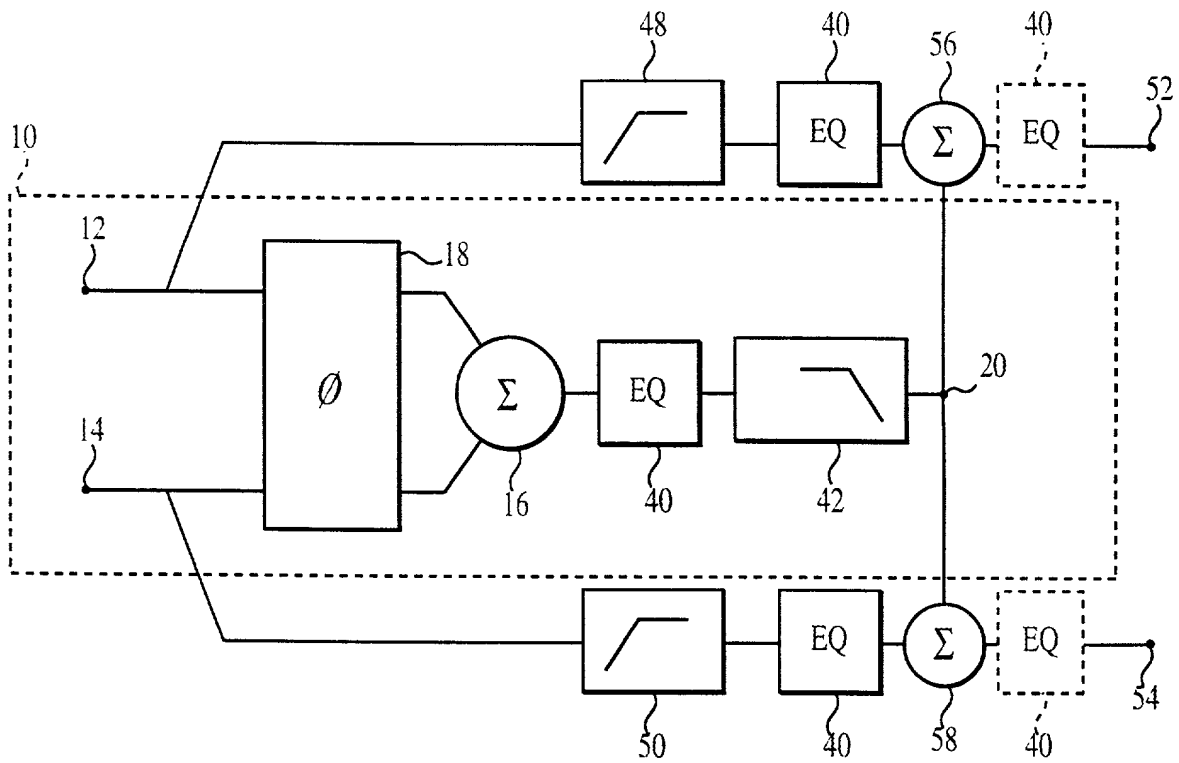


FIG. 3c

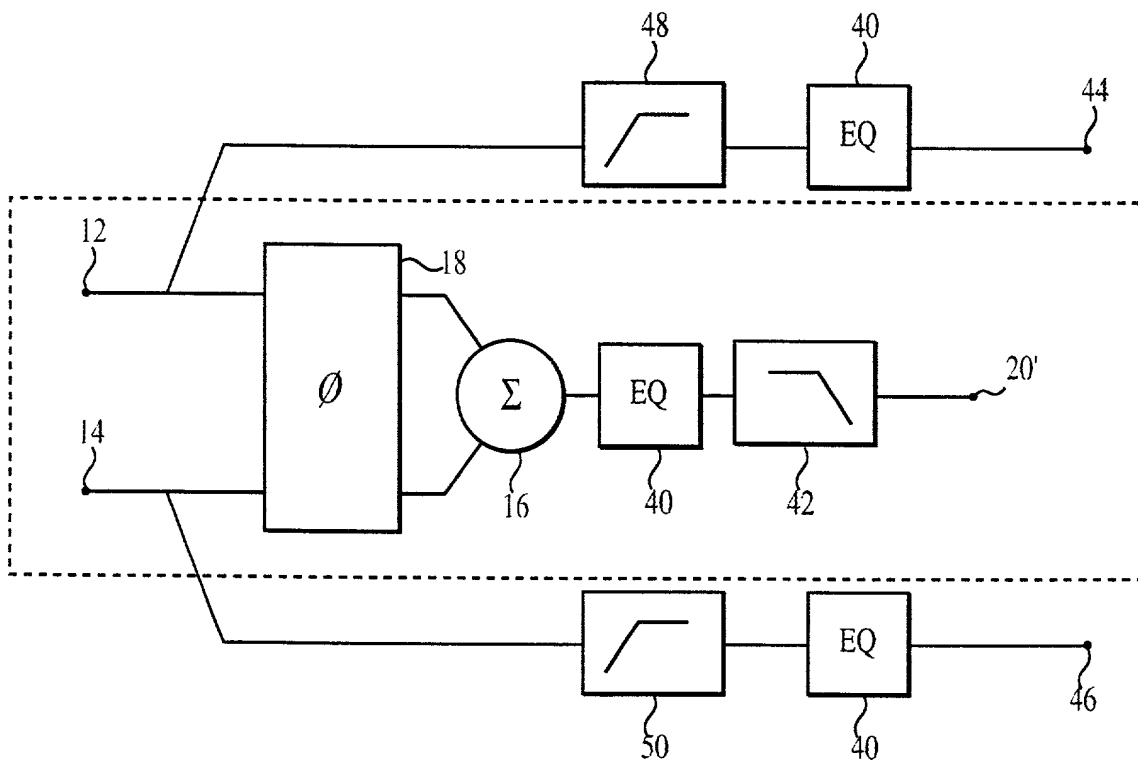


FIG. 3d

FIG. 4a is a schematic diagram of a circuit for processing an input signal. The circuit includes two input channels, L and R, each with a low-pass filter and a summing junction. The L channel filter has a time constant of $(T_1 - 1/5) / (T_1 + 1/5)$ and a cutoff frequency of 20 Hz. The R channel filter has a time constant of $(T_2 - 1/5) / (T_2 + 1/5)$ and a cutoff frequency of 200 Hz. The summing junctions are labeled "SUM AND DIVIDE BY 2". The output of the L channel is connected to a "CORRECTION CIRCUIT" which includes an integrator and an inverter. The output of the R channel is connected to the same "CORRECTION CIRCUIT". The "CORRECTION CIRCUIT" also includes a feedback loop with a time constant of $\sqrt{(T_1 T_2 + 1/5)}$.

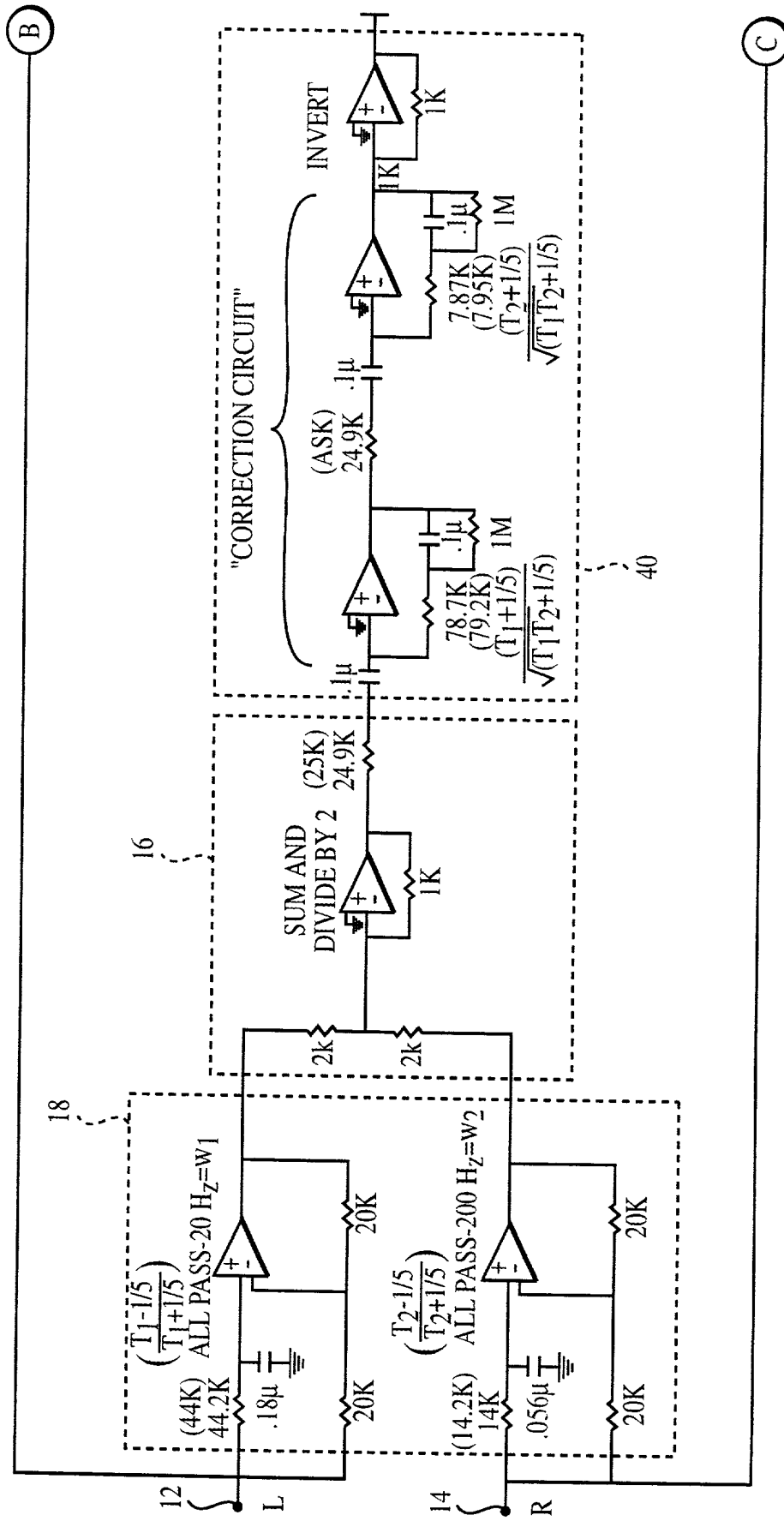


FIG. 4a

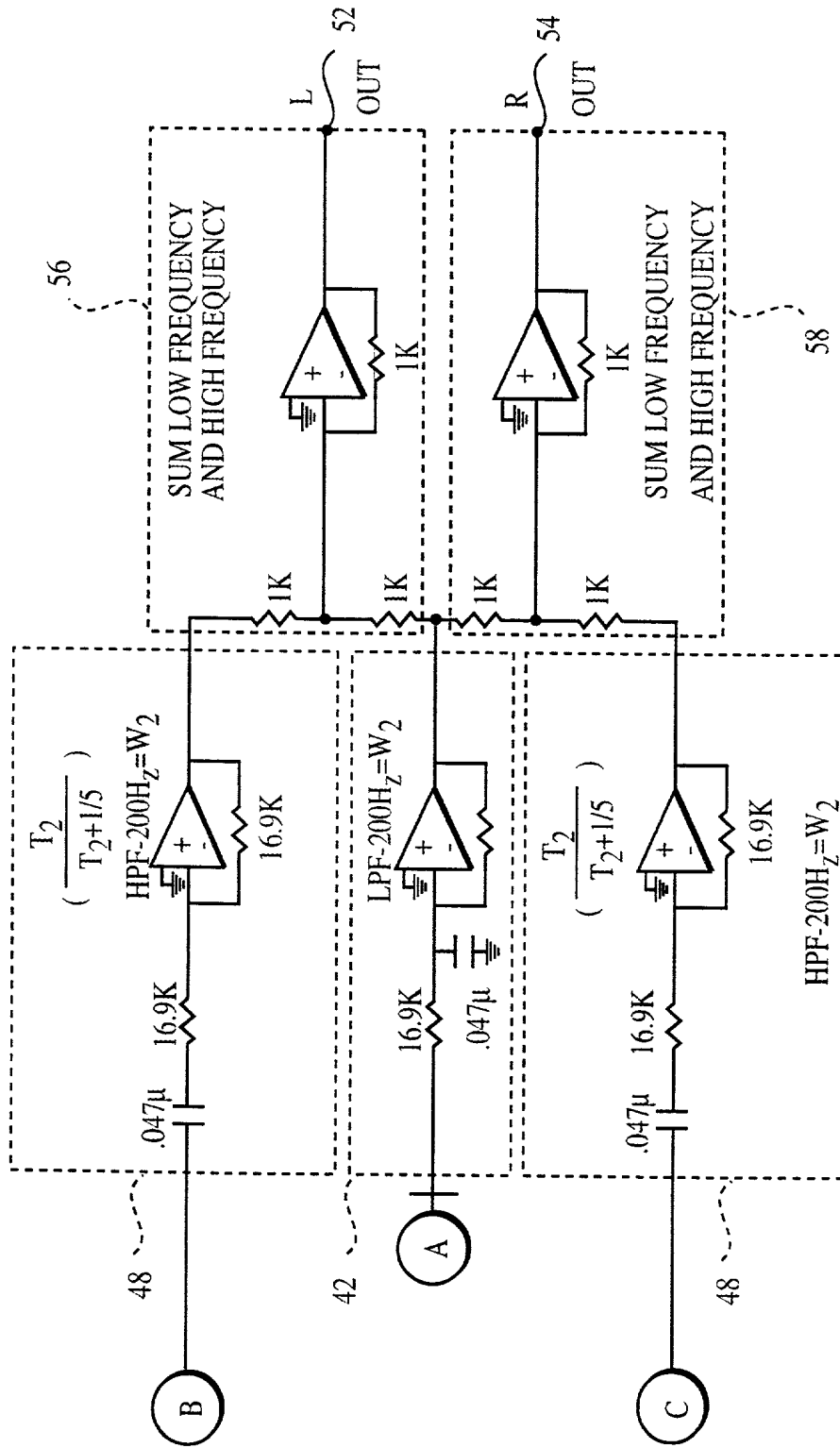


FIG. 4b

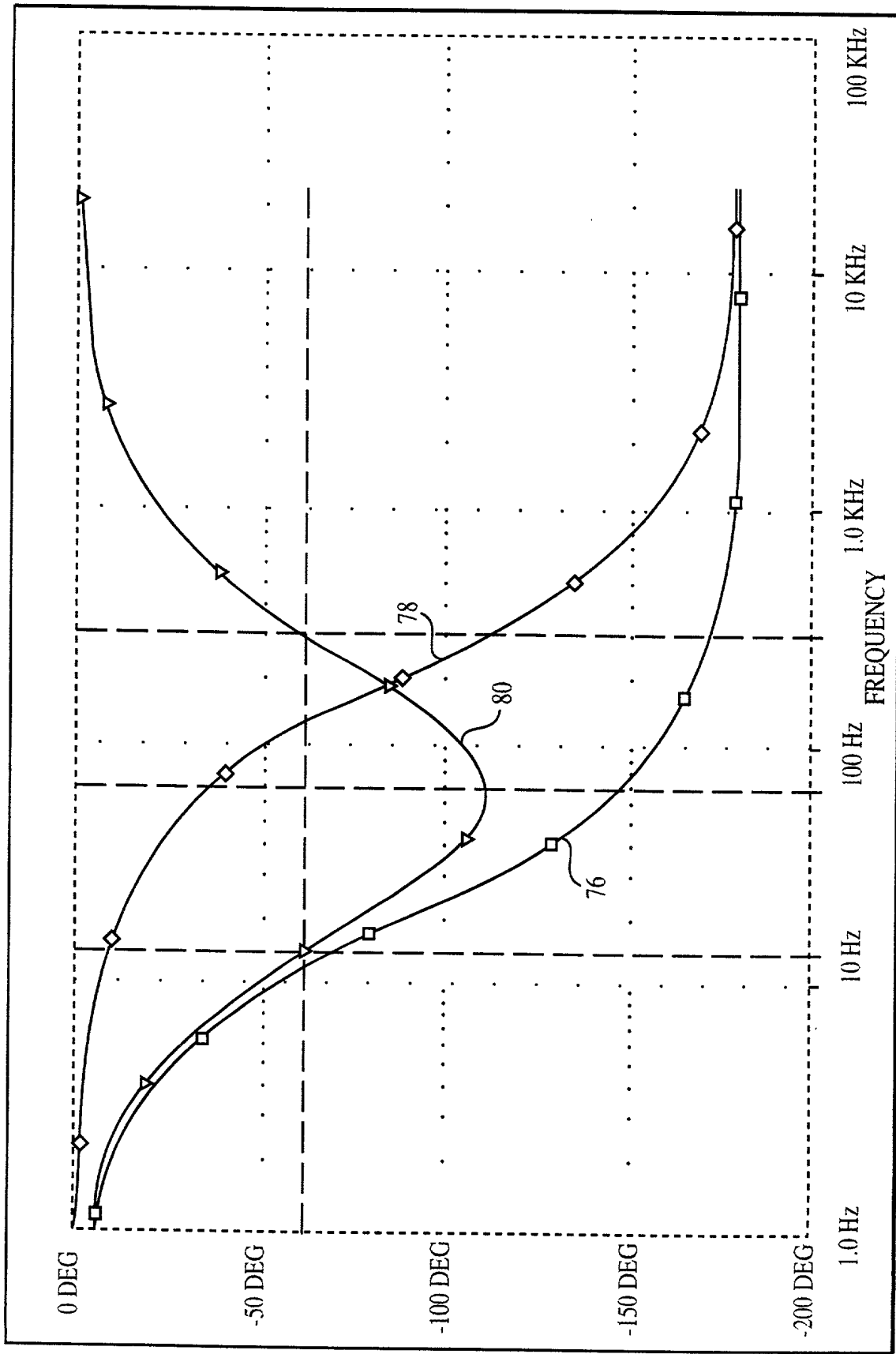


FIG. 5a

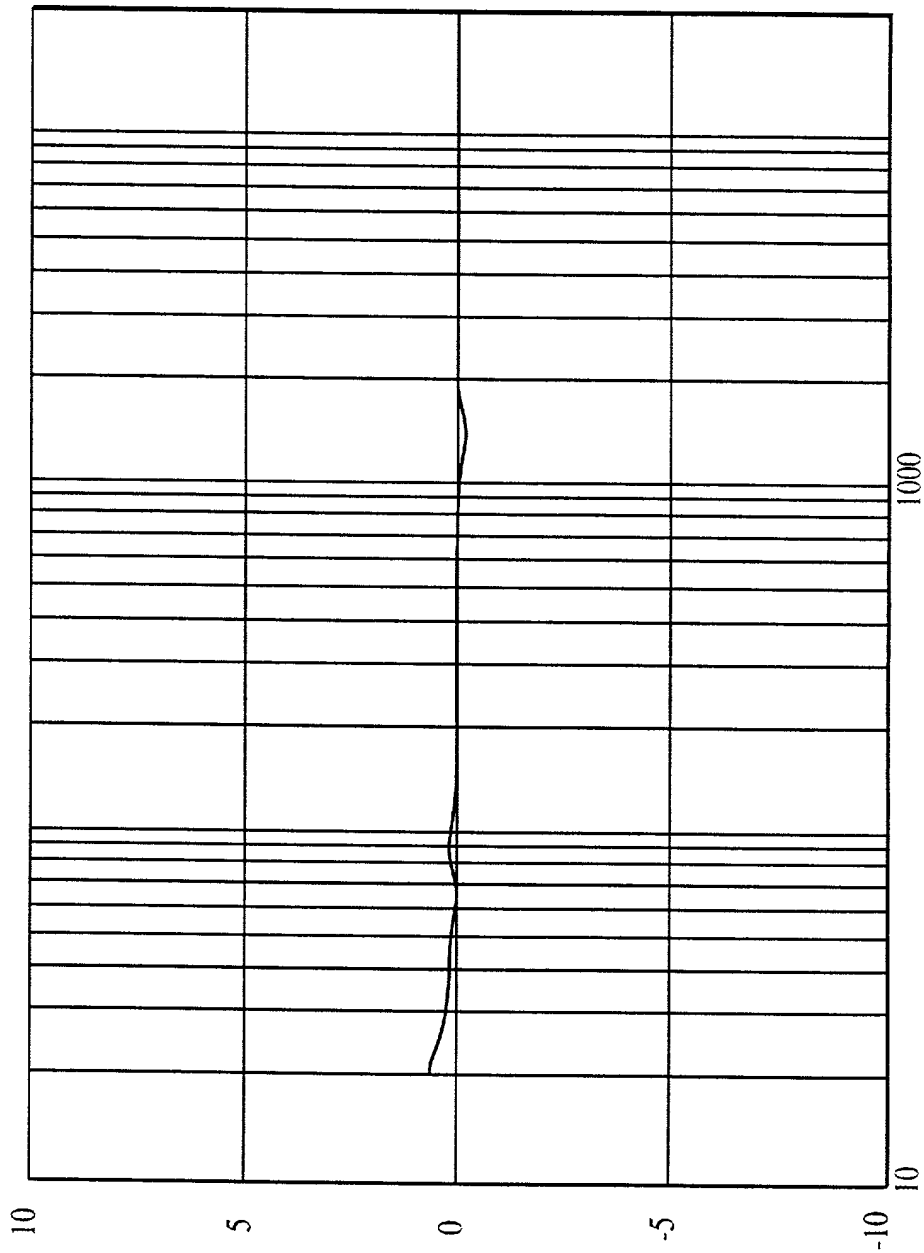


FIG. 5b

FIG. 6 is a block diagram of a stereo system 10, showing the interconnection of various components including a central processing unit 10, a left channel processor 23, a right channel processor 28, and a central summing junction 20.

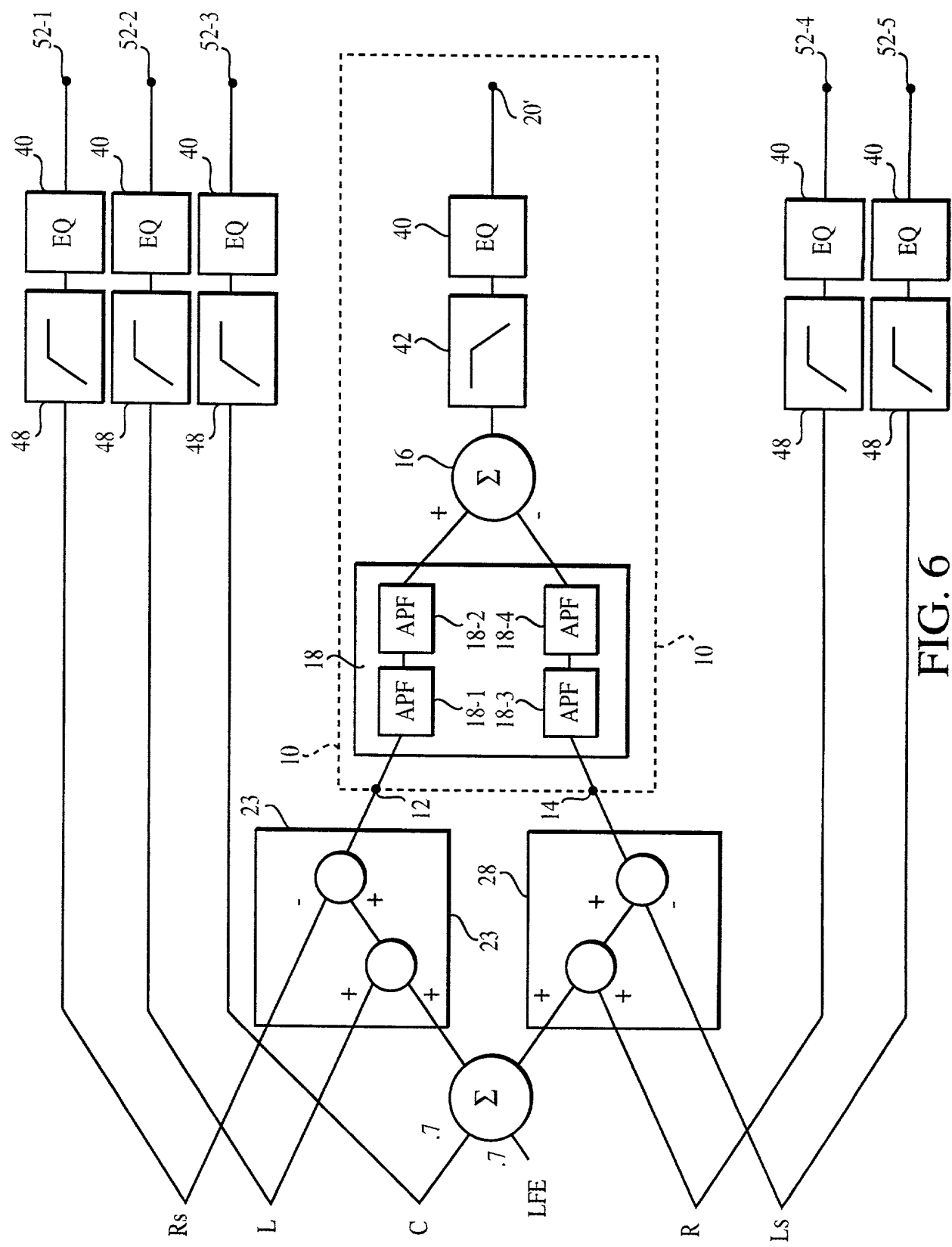
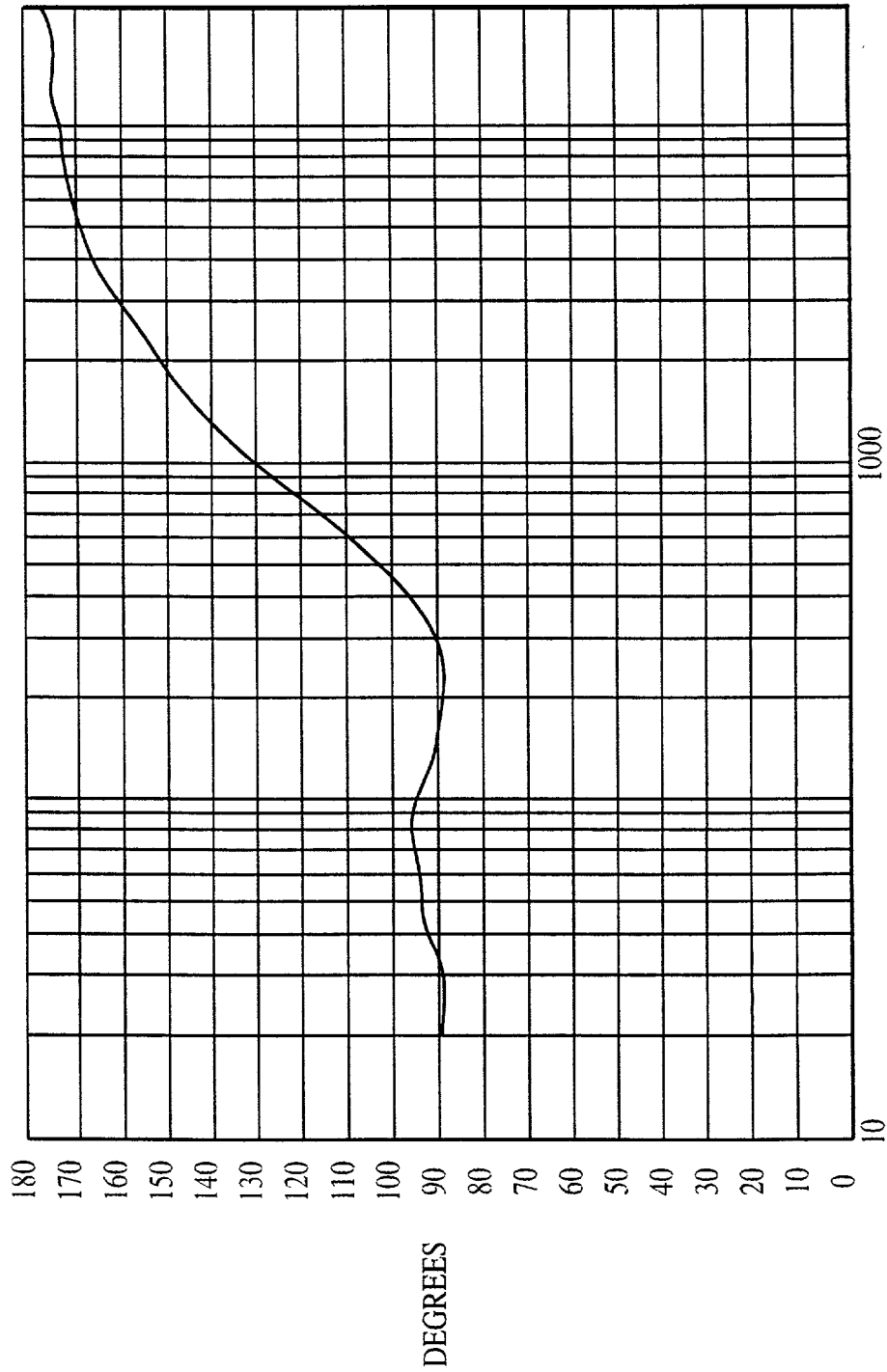


FIG. 6

FIG. 7a



Hz

FIG. 7a

FIG. 7b

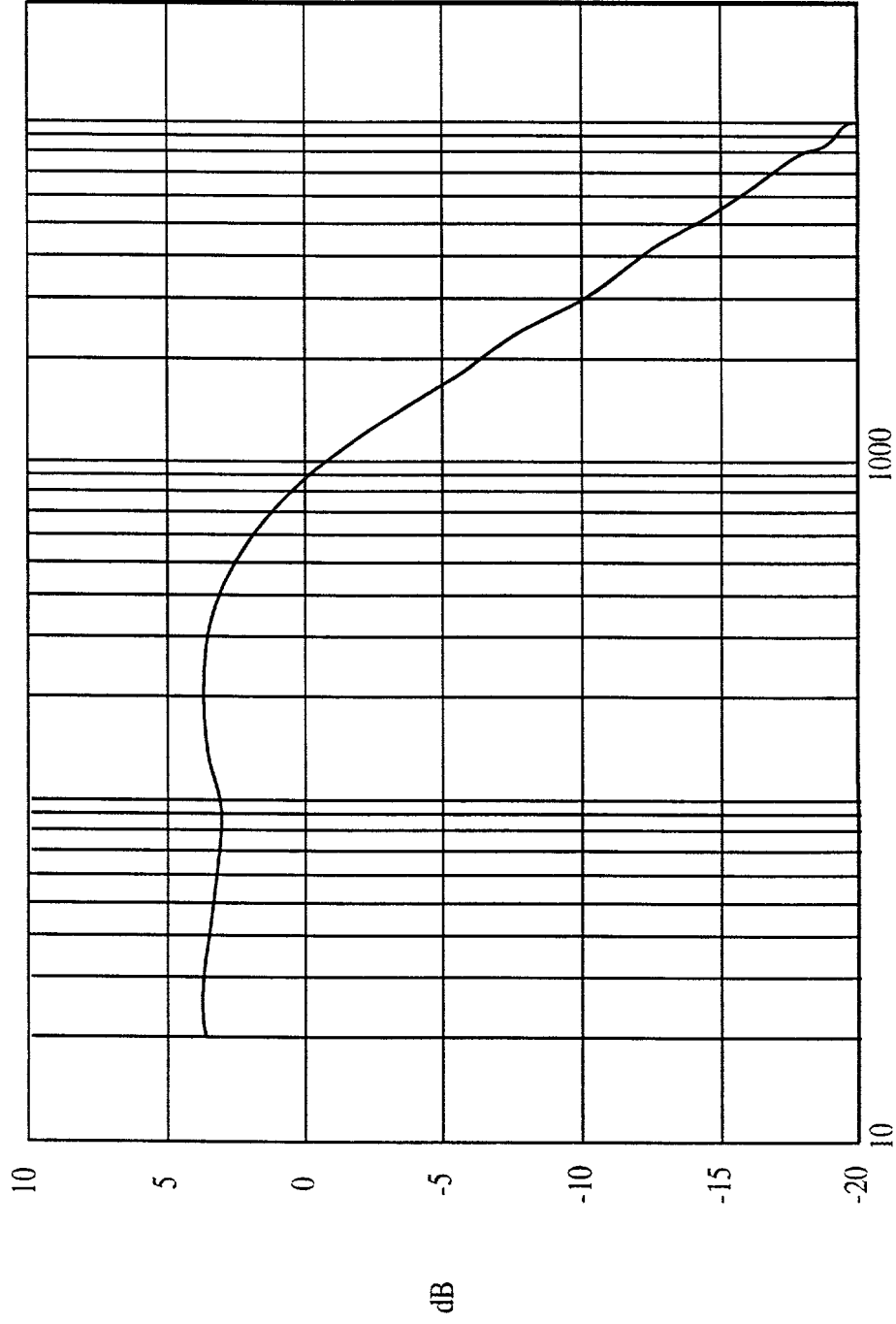


FIG. 7b

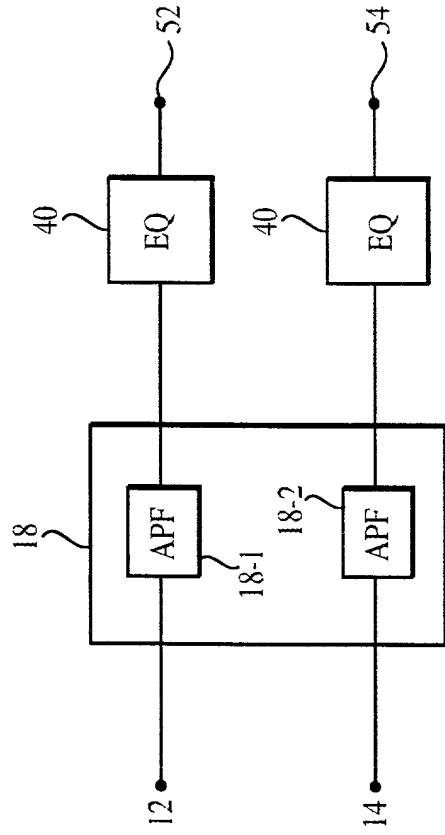


FIG. 8a

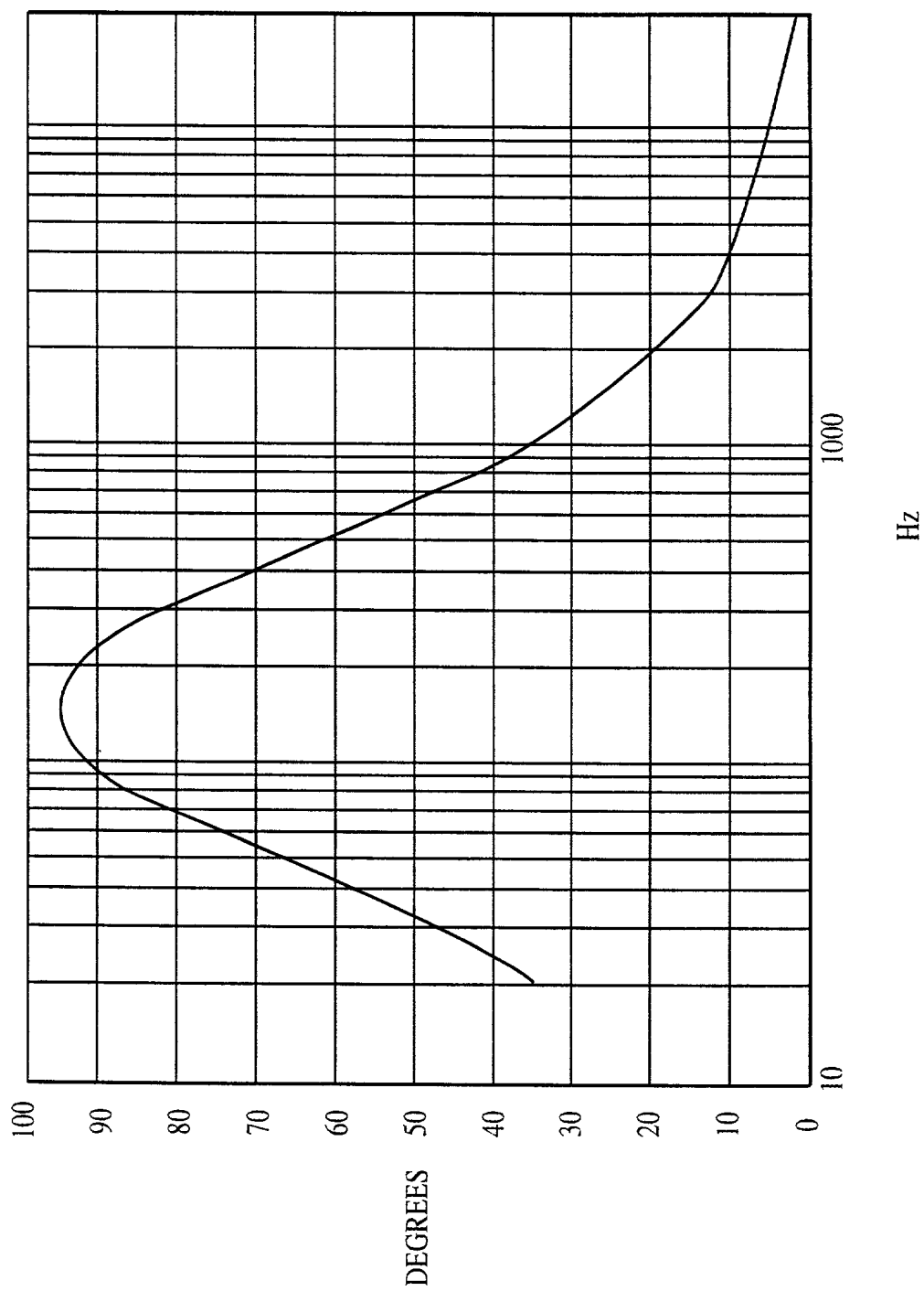


FIG. 8b

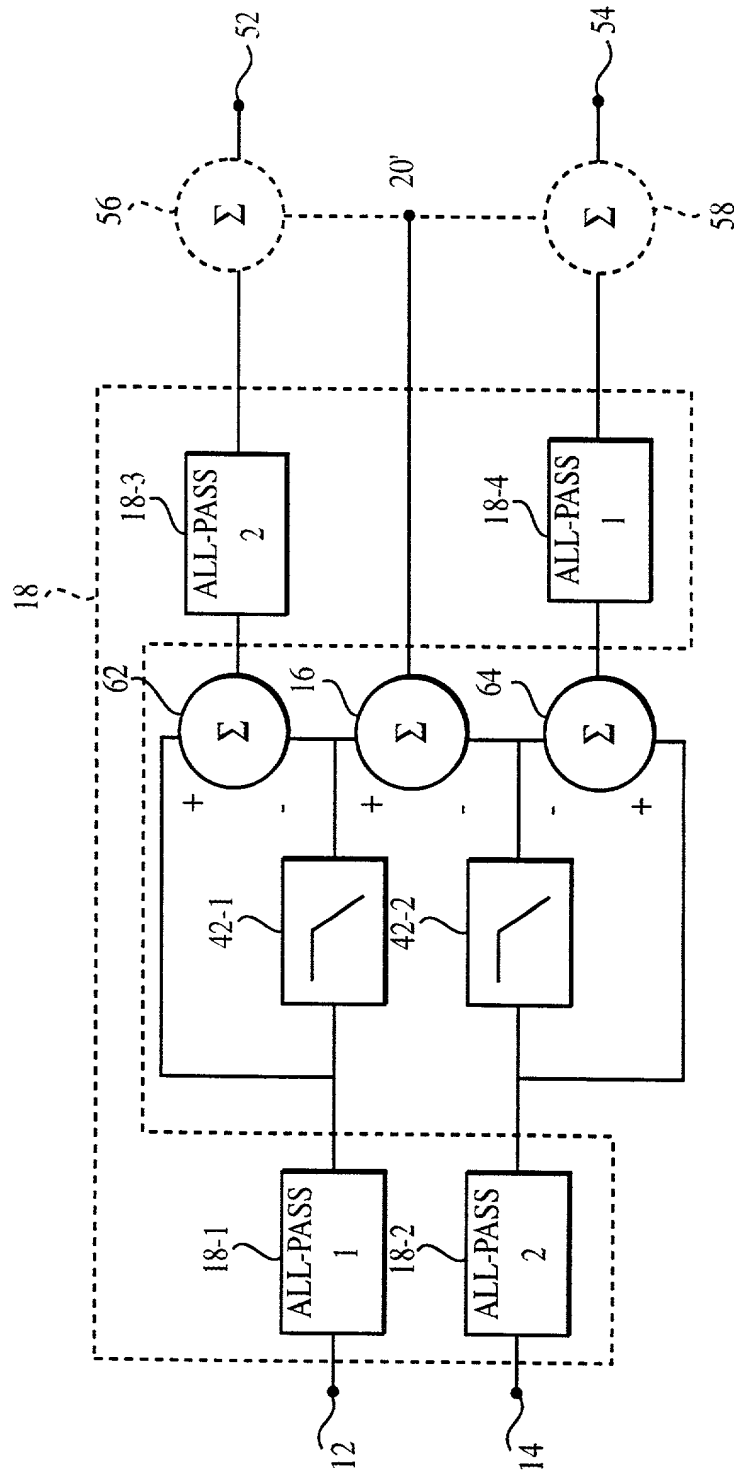


FIG. 9